IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF PENNSYLVANIA

AGERE SYSTEMS INC.,	:	CIVIL ACTION
Plaintiffs,	:	
	:	
v.	:	NO. 02-864
	:	
ATMEL CORPORATION,	:	
Defendant.	:	

MEMORANDUM

LEGROME D. DAVIS, J. MAY____, 2003

I. INTRODUCTION

Plaintiff Agere Systems Inc. ("Agere") filed this patent infringement suit against Defendant Atmel Corporation ("Atmel") alleging that Atmel is infringing United States Patent No. 5,227,335 ("the '335 patent"), U.S. Patent No. 6,323,126 ("the '126 patent"), U.S. Patent No. 5,102,827 ("the '827 patent"), U.S. Patent No. 5,149,672 ("the '672 patent"), and U.S. Patent No. Re. 34,269 ("the '269 patent"). The five patents-in-suit assert claims in the field of semiconductor integrated circuits: four of the patents contain claims that concern processes for fabricating a semiconductor integrated circuit, and the fifth contains claims that concern a particular metal frame structure for packaging semiconductor integrated circuits.

On December 5 and 6, 2002, a Markman hearing was held on the issue of claim construction, at which the parties presented evidence and offered expert testimony as to the

proper construction of the disputed claim language in the claims at issue. The parties have also submitted a series of briefs and proposed claim constructions to the Court, all of which have been considered by the Court in making the claim constructions that follow. In addition, the parties have submitted a list of the claim terms which are not in dispute and, unless otherwise noted herein, the Court has not construed these undisputed terms. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997) ("Claim construction is a matter of resolution of *disputed* meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement." (emphasis added)).

For purposes of construing each disputed claim term, the parties have submitted numerous arguments and have pointed to many portions of the intrinsic and extrinsic record. While the Court has considered all of the arguments and citations of the parties, the Court may not reiterate all of them in full for each claim term.

II. THE LAW OF PATENT CLAIM CONSTRUCTION

"The Constitution empowers Congress '[t]o promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries.'" Markman v. Westview Instruments, Inc., 517 U.S. 370, 373 (1996) (quoting U.S. Const. Art. I, § 8, cl. 8). In general, "a patent must describe the exact scope of an invention and its manufacture to 'secure to [the patentee] all to which he is entitled, [and] to apprise the public of what is still open to them.'" Id. (citation omitted). This is accomplished through (1) the specification of the patent, which should describe the invention "in such full, clear, concise, and exact terms as to enable any person skilled in the art . . . to make

and use" the invention, and (2) the claims of the patent, which should "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶¶ 1, 2; Markman, 517 U.S. at 373. In a patent lawsuit, the plaintiff generally alleges that the defendant has infringed the plaintiff's patent by making, using, offering to sell, or selling the patented invention without authority within the United States during the term of the patent. See 35 U.S.C. § 271(a); Markman, 517 U.S. at 374. "Victory in an infringement suit requires a finding that the patent claim 'covers the alleged infringer's product or process,' which in turn necessitates a determination of 'what the words in the claim mean.'" Markman, 517 U.S. at 374 (citations omitted).

In Markman, the Supreme Court held that the construction of patent claims is exclusively within the province of the court to determine as a matter of law. Id. at 372. "It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." Id. "In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term." Id. at 1583. Reliance on extrinsic evidence is proper only if an analysis of the intrinsic evidence fails to resolve ambiguities in a disputed claim term. See id.

A. Claim Language

The starting point for defining the scope of a patented invention is to examine the claims and to give them their ordinary and accustomed meaning as understood by one of ordinary skill

in the art at the time of the invention. See Bell Atlantic Network Services, Inc. v. Covad Comm. Group, Inc., 262 F.3d 1258, 1267 (Fed. Cir. 2001); Markman v. Westview Instruments, Inc., 52 F.3d 967, 986 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370. "[I]n determining the ordinary meaning of a technical term, courts are free to consult scientific dictionaries and technical treatises at any time." Dow Chem. Co. v. Sumitomo Chem. Co., Ltd., 257 F.3d 1364, 1372-73 (Fed. Cir. 2001). Terms that are not used in a technical sense may be construed through reference to a general purpose dictionary. See AFG Industries, Inc. v. Cardinal IG Co., Inc., 239 F.3d 1239, 1248 (Fed. Cir. 2001).

> Dictionaries, encyclopedias and treatises, publicly available at the time the patent is issued, are objective resources that serve as reliable sources of information on the established meanings that would have been attributed to the terms of the claims by those of skill in the art. Such references are unbiased reflections of common understanding not influenced by expert testimony or events subsequent to the fixing of the intrinsic record by the grant of the patent, not colored by the motives of the parties, and not inspired by litigation. Indeed, these materials may be the most meaningful sources of information to aid judges in better understanding both the technology and the terminology used by those skilled in the art to describe the technology.

Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202-03 (Fed. Cir. 2002).

"Generally, there is a 'heavy presumption' in favor of the ordinary meaning of claim language as understood by one of ordinary skill in the art." Bell Atlantic, 262 F.3d at 1268. This presumption may be overcome in one of four ways:

> First, the claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history. Second, a claim term will not carry its ordinary meaning if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular

> embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention.
>
> Third, . . . a claim term also will not have its ordinary meaning if the term "chosen by the patentee so deprive[s] the claim of clarity" as to require resort to the other intrinsic evidence for a definite meaning. Last, as a matter of statutory authority, a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto, if the patentee phrased the claim in step- or means-plus-function format.

CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d 1359, 1366-67 (Fed. Cir. 2002).

Thus, where the claim language is clear on its face, the remaining intrinsic evidence is considered only to determine whether a deviation from that clear definition is specified, either because the patentee set forth a definition of the disputed claim term, or because the patentee distinguished the term from prior art. See Interactive Gift Express, Inc. v. Compuserve Inc., 256 F.3d 1323, 1331 (Fed. Cir. 2001). On the other hand, where the claim language is not clear on its face, the remaining intrinsic evidence is examined more broadly with an eye toward resolving any ambiguities. See id.

B. Specification

"[I]t is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning." Vitronics Corp., 90 F.3d at 1582. The specification may act as a dictionary when it expressly or implicitly defines terms used in the claims. Id. (citing Markman, 52 F.3d at 979). "In such a case, the definition selected by the patent applicant controls," and the court construing the claims must refer to the written description "because only there is the claim term defined as it is used by the patentee." Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1249 (Fed. Cir. 1998). "The law provides a patentee with this opportunity because the public may not be schooled in the terminology of the

technical art or there may not be an extant term of singular meaning for the structure or concept that is being claimed." Id. Also, where a claim term lends itself to several common meanings, a court may resort to the specifications because "the patent disclosure serves to point away from the improper meanings and toward the proper meaning." Id. at 1250.

Although the specification may provide guidance in construing the meaning of claim terms, it is improper to read limitations appearing in the specification into claims. See, e.g., Intervet America, Inc. v. Kee-Vet Laboratories, Inc., 887 F.2d 1050, 1053 (Fed. Cir. 1989); Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 867 (Fed. Cir. 1985) ("Generally, particular limitations or embodiments appearing in the specification will not be read into the claims."), *overruled on other grounds*, Nobelpharma AB v. Implant Innovations, Inc., 141 F.3d 1059 (Fed. Cir. 1998). This somewhat subtle distinction has been explained in the following way:

> "The claims of the patent provide the concise formal definition of the invention. . . . It is to these wordings that one must look to determine whether there has been infringement. Courts can neither broaden nor narrow the claims to give the patentee something different than what he has set forth. No matter how great the temptations of fairness or policy making, courts do not rework claims. They only interpret them."
>
> In accordance with that instruction, this court has consistently adhered to the proposition that courts "cannot alter what the patentee has chosen to claim as his invention."
>
> It is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim. But this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By "extraneous," we mean a limitation read into a claim from the specification wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim. "Where a specification does not require a limitation, that limitation should not be read from the specification into the claims."

E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed. Cir. 1988) (citations omitted).

C. Prosecution History

The prosecution history "contains the complete record of all the proceedings before the Patent and Trademark Office, including any express representations made by the applicant regarding the scope of the claims." Bell Atlantic, 262 F.3d at 1268. This history must be examined to determine whether or not there were any express representations made in obtaining the patent regarding the scope and meaning of the claims, such as in an amendment to the claim or in an argument to overcome or distinguish a reference. See id. A patentee may be found to have relinquished a potential claim construction where he has made such express representations in obtaining the patent. See id. "Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers." Southwall Techs., Inc. v. Cardinal IG, Co., 54 F.3d 1570, 1576 (Fed. Cir. 1995).

D. Extrinsic Evidence

It is well-established that extrinsic evidence may be used in construing claim terms only under certain circumstances:

> Finally, if the meaning of the claim limitation is apparent from the intrinsic evidence alone, it is improper to rely on extrinsic evidence other than that used to ascertain the ordinary meaning of the claim limitation. However, in the rare circumstance that the court is unable to determine the meaning of the asserted claims after assessing the intrinsic evidence, it may look to additional evidence that is extrinsic to the complete document record to help resolve any lack of clarity. This additional extrinsic evidence includes such evidence as expert testimony, articles, and inventor testimony. This extrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand, or limit the

> claim language from how it is defined, even by implication, in the specification or file history.

Bell Atlantic, 262 F.3d at 1258-59.

III. GENERAL BACKGROUND INFORMATION

An integrated circuit consists of microscopic components (including electronic switches or transistors) and electrical interconnections which are integrated into a wafer-thin piece of material referred to as a "chip." The material that is used for these chips is known as a "semiconductor" material, of which silicon is perhaps the most well-known example. Semiconductor material is used because its properties can be modified to make it electrically conductive, or to make it perform as an insulator. Thus, a "semiconductor integrated circuit" is a small chip made of a semiconductor material that contains a large number of microscopic components electrically interconnected so as to achieve a particular set of functions.

The fabrication of a semiconductor integrated circuit generally begins with a semiconductor "substrate," a thin disk or wafer of semiconductor material (often silicon) that is typically about eight inches in diameter and about one millimeter or less in thickness. Certain features of the microscopic components that will ultimately be part of the circuitry on the integrated circuit are fabricated below the surface of the substrate, and others are fabricated above the surface of the substrate. Multiple layers may then be fabricated on top of the substrate and these components. In order to prevent leakage of charge particles between levels, an insulating layer of material called a "dielectric" is used. As jointly defined by the parties, "dielectric" means "a material that exhibits little or no electrical conductivity and that can act as a good electrical insulator." Second Revised Joint Statement of Disputed Claim Terms ("Joint

Statement of Claim Terms") at 1. Typically, certain components below an insulating layer of dielectric are meant to be electrically connected to levels above the dielectric. In order to expose components below a layer of dielectric and allow them to become electrically connected, certain portions of the dielectric must be selectively removed. This removal is accomplished through a series of steps.

First, the entire surface of the dielectric is covered with a layer of a light-sensitive compound known as "photoresist." Second, in the areas where the dielectric needs to be removed, the photoresist is selectively illuminated by passing light through a "mask" (a sheet or plate with holes in selected locations) and projecting the mask image onto the surface of the photoresist. The light causes a chemical alteration in the exposed areas of the photoresist. Third, the entire chip is subjected to a process that washes away the altered photoresist, thereby exposing the underlying dielectric in certain areas while leaving the unaltered photresist in place shielding the underlying dielectric in other areas. Fourth, the entire surface of the chip is exposed to a substance known as an "etchant," which has no significant effect on the areas that remain covered by photoresist, but which chemically removes the dielectric from the areas where the dielectric has been exposed. Finally, the wafer is cleaned and stripped of the remaining photoresist.

The openings in the dielectric layer that result from this process are created above certain components to allow them to be electrically connected. A subsequent sequence of operations is then used to form "contacts." Each of the openings is filled with a conductive material such as a metal. Then a layer of metal is deposited over the entire surface of the chip, such that all of the contact terminals on all of the components on the chip are electrically connected to each other by

the metal layer. Because only certain connections are desired between certain components, a sequence of steps must be performed to remove the undesired portions of the metal layer. This is, once again, achieved through the multi-step process described above.

Thus are openings, contacts, and interconnections within a single layer formed. Modern semiconductor integrated circuits often contain multiple layers, and the basic sequence of steps for creating each additional layer is effectively the same as described above. Finally, when all of the necessary layers have been formed, the wafer is separated into multiple rectangular chips, each constituting an identical semiconductor integrated circuit. Each chip is then packaged and may be used in various products.

IV. CONSTRUCTION OF THE CLAIMS IN THE ‘335 PATENT

A. Background to the ‘335 Patent

Tungsten metal may be used as the conductive material to fill the openings that are formed in a dielectric layer as described above. The advantage of using tungsten over other metals such as aluminum is that tungsten can be used in smaller (or more narrow or shallow) openings, allowing smaller chips to be fabricated. However, tungsten generally does not adhere well to dielectric material. The ‘335 patent is directed to a process intended to rectify this problem by depositing a “glue layer” (which contains an electrically conducting material) between the dielectric and the tungsten which allows the tungsten to adhere to the dielectric.

Specifically, the ‘335 patent is directed to a process whereby, after the openings have been created in the dielectric layer, a glue layer is deposited over the entire surface of the wafer and then a tungsten layer is deposited over the glue layer. Then a process is used to remove the portions of the tungsten and glue layers that are not within an opening, leaving a relatively flat

surface of dielectric in which the openings are now filled with tungsten as well as a layer of glue between the tungsten and the dielectric. Claims 1 through 8 and claim 10 of the '335 patent are at issue in this lawsuit.

B. The '335 Claims

The '335 patent sets forth the following claims (with the disputed claim terms underlined):

> 1. A method of fabricating an integrated circuit comprising the steps of:
>
> patterning a dielectric layer to form holes which expose the underlying material, said exposed underlying material comprises an electrically conducting material;
>
> depositing a glue layer covering said dielectric and said exposed underlying material;
>
> depositing a tungsten layer by chemical vapor deposition, said tungsten layer covering said glue layer on said dielectric and said exposed material;
>
> CHARACTERIZED IN THAT said glue layer comprises at least one member selected from the group consisting of conducting nitrides.
>
> 2. A method as recited in claim 1 in which said material comprises said silicon surface.
>
> 3. A method as recited in claim 1 in which said material comprises a metallic silicide.
>
> 4. A method as recited in claim 1 further comprising etching said tungsten and said glue layer to form a planar surface of said dielectric and said tungsten in said hole, said tungsten being etched before said glue layer.
>
> 5. A method as recited in claim 4 in which said conducting nitride consists essentially of TiN.
>
> 6. A method as recited in claim 1 in which said dielectric comprises silicon dioxide.
>
> 7. A method as recited in claim 1 in which said W layer is deposited by low pressure chemical vapor deposition.
>
> 8. A method as recited in claim 7 in which said deposition uses WF_6 and H_2.
>
> 9. A method as recited in claim 8 in which said glue layer comprises a conducting nitride.

> 10. A method as recited in claim 8 in which said conducting nitride comprises TiN.
>
> 11. A method as recited in claim 1 further comprising the step of patterning said tungsten and said glue layer.

'335 Patent at col. 5:22 through col. 6:29.

1. "patterning"

Agere argues that the term "patterning" should be construed as "performing the process of lithography (producing a pattern that covers portions of the substrate with resist) followed by etching (selective removal of material not covered by resist) or otherwise transferring the pattern into the substrate." Atmel argues that the term "patterning" should be construed as "the process steps of covering a semiconductor wafer with photoresist, selectively exposing portions of the photoresist to illumination through a mask, and then washing away the photoresist in selected areas." The essential difference between the parties' constructions is that Agere contends that patterning includes the step of etching, while Atmel contends that patterning does not include the step of etching. The Court concludes that Agere's proposed construction is the proper construction for the following reasons.

First, claim 1 expressly states that the patterning contemplated by the patentee will result in the formation of "holes" in the dielectric exposing the underlying material. Both parties agree that the step of etching is necessary to form holes, and Atmel does not appear to dispute that patterning, according to Atmel's own proposed construction (which excludes the step of etching), would not result in holes in the dielectric. Atmel contends, however, that to the extent that claim 1 does not make sense if Atmel's construction is adopted, the claim is poorly drafted and should not be redrafted by the Court. The Court finds that because claim 1 expressly indicates that

patterning will result in the formation of holes in the dielectric, it is clear that a person of ordinary skill in the art would have understood the term patterning as used in claim 1 to include the step of etching.

In addition, the Court has referred to the "Comprehensive Dictionary of Electrical Engineering," which provides precisely the definition for patterning offered by Agere. See Comprehensive Dictionary of Electrical Engineering 475 (Phillip A. Laplante ed., 1999). Furthermore, Agere's expert witness testified that this definition would have been the definition used by a person of ordinary skill in the art at the time of the invention. See Transcript of Hearing on December 5, 2002 ("Tr. 12/5/02") at 33-34.

The Court has also examined the remaining intrinsic evidence (the specification and the prosecution history) to determine whether a deviation from this clear definition of patterning is expressed. See Interactive Gift, 256 F.3d at 1331. Atmel points to the specification which, in one instance, describe steps that "pattern" the dielectric and steps that "etch" the dielectric in such a way as to imply that they are distinct steps. See '335 Patent at col. 3:51-53. Also, Atmel points to one instance in which the specification appears to use the word "patterned" to refer to resist before etching has occurred. See '335 Patent at col. 5:10-13. However, an important, albeit subtle, distinction must be recognized here. Although the word "pattern" may be used in the specification in certain instances to refer to a step that does not include etching, and although the word "patterned" may be used in the specification in certain instances to refer to resist before it has been etched, all of the intrinsic evidence, including the claim language and the specification, shows that the word "patterning" (as opposed to "pattern" or "patterned") is consistently used in such a way as to include the step of etching. For example, the specification

in one instance states that "[t]he strong adhesion provided by thin glue layers is useful for patterning W interconnects," '335 Patent at col. 5:6-7, and, as explained by Agere's expert witness, the formation of "interconnects" requires the step of etching, see Tr. 12/05/02 at 38.

Thus, according to all of the intrinsic evidence, "patterning" as used in the claims of the '335 patent occurs when one first patterns the dielectric (producing a patterned resist) and then etches the dielectric. Accordingly, the Court construes "patterning" as "performing the process of lithography (producing a pattern that covers portions of the substrate with resist) followed by etching (selective removal of material not covered by resist) or otherwise transferring the pattern into the substrate."

2. "holes"

Agere argues that the term "holes" should be construed as "hollow places in a solid body or mass." Atmel argues that the term "holes" should be construed as "contact holes, that is, openings in the first dielectric layer that expose the silicon surface (i.e., the silicon substrate) or the conducting material at the silicon surface." The essential difference between the parties' constructions is that Atmel contends the term "holes" only applies to openings in the first dielectric layer, which openings would necessarily expose the silicon surface of the wafer, or the conducting material at the silicon surface of the wafer. Thus, Atmel apparently contends that the term "holes" would not apply to openings in dielectric layers that are positioned above the first dielectric layer (which would expose some previously-created metal contact rather than exposing the silicon surface of the wafer or the conducting material at the silicon surface of the wafer). The Court concludes that Agere's proposed construction is the proper construction for the following reasons.

Agere's proposed construction comports with the ordinary meaning of the term "hole." According to the "Random House Dictionary of the English Language," one of the definitions of the word "hole" (and the definition most appropriate to this context) is "a hollow place in a solid body or mass; a cavity." See Random House Dictionary of the English Language 911 (2d ed. 1987). Moreover, Atmel's construction would incorporate into claim 1 a restriction that is set forth in the subsequent dependent claims. Dependent claim 2 is directed toward "[a] method as recited in claim 1" in which the underlying material exposed by the "holes" in the dielectric layer is specified as being the silicon surface of the wafer, and dependent claim 3 is directed toward "[a] method as recited in claim 1" in which the underlying material exposed by the "holes" in the dielectric layer is specified as being a metallic silicide. See '335 Patent at col. 6:7-10. Thus, dependent claims 2 and 3 illustrate that where the patentee intended to specify or limit the type of material exposed by the "holes," the patentee did so explicitly. Therefore, since claim 1 does not on its face specify or limit the type of material exposed by the "holes," it would be inappropriate to limit the term "holes" as applying only to openings in the first dielectric layer which expose the silicon surface of the wafer or the conducting material at the silicon surface of the wafer. Indeed, "[i]t is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim in determining either validity or infringement." SRI Int'l v. Matsushita Elec. Corp. of American, 775 F.2d 1107, 122 (Fed. Cir. 1985).

There is a heavy presumption that a claim term carries its ordinary and customary meaning. CCS Fitness, 288 F.3d at 1366. In order to deviate from the ordinary and customary meaning, Atmel must show that the intrinsic evidence establishes that the patentee demonstrated

an intent to do so either by setting forth some other specific definition of the disputed claim term, or by distinguishing the term from prior art. See Interactive Gift, 256 F.3d at 1331. However, an examination of the specification only provides further support for Agere's proposed construction. In addition to contemplating that "[t]he glue layer film may be deposited, through openings in the dielectric, directly on the silicon or on a conducting material, such as a silicide, overlying the silicon," '335 Patent at col. 3:7-10, the specification notes that the deposition process may be used for other purposes, such as "to form interconnects,"[1] '335 Patent at col. 5:3-6, and that "[t]he use of A1 [tungsten] *is particularly suited for upper levels in multilevel metallization schemes* where junction spiking is not a consideration," '335 Patent at col. 5:14-16 (emphasis added). Thus, it appears that the patentee specifically contemplated using the deposition process to fill not only openings in the first dielectric layer, but also openings in layers other than the first dielectric layer.

In summary, Agere's proposed construction of the term "holes" comports with the ordinary meaning of the word, the claim language, and the remaining intrinsic evidence. Accordingly, the Court construes the term "holes" as "hollow places in a solid body or mass."

3. "glue layer"

[1] Atmel argues that the term "interconnect" does not refer to openings in upper-level dielectric layers, but rather refers to a structure that connects two points on the same level to one another. However, the specification makes clear that, at least according to the patentee, the term "interconnect" means "the lines and *windows* used to connect devices," and, according to the patentee, the term "window," in turn, can be used to mean *either* (1) *only* "the openings to the source, gate, or drain electrodes" (*i.e.*, openings in the first dielectric layer), in which case "opening[s] between levels in multilevel metal structures" are distinguished as "vias," or (2) *both* "the openings to the source, gate, or drain electrodes" *and* "the opening[s] between levels in multilevel metal structures," in which case the terms "windows" and "vias" are interchangeable. See '335 Patent at col. 1:17-28.

Agere argues that the term "glue layer" should be construed as "a layer, composed of one or more materials, that promotes adhesion between an underlying dielectric region and a subsequently-deposited tungsten layer." Atmel argues that the term "glue layer" should be construed as "a layer of material of a single composition that adheres well to the dielectric layer, to the tungsten layer that is subsequently deposited, and to the exposed material at the bottom of the contact hole." There are two essential differences between the parties' constructions: (1) Agere contends the glue layer may contain more than one material, while Atmel contends the glue layer must be composed of only a single material; and (2) Atmel contends that the glue layer must adhere well to the exposed material at the bottom of the contact hole, in addition to adhering well to the dielectric and the tungsten, while Agere contends the glue layer need only promote adhesion between the dielectric and the tungsten.

As to the composition of the glue layer, Claim 1 itself expressly states that "said glue layer comprises *at least one member* selected from the group consisting of conducting nitrides." '335 Patent at col. 6:4-6 (emphasis added). Similarly, the specification states that "[t]he glue layer comprises *at least one material* selected from the group consisting of A1 and conducting nitrides such as TiN." Id. at col. 3:67 through col. 4:1 (emphasis added). This language clearly implies that the glue layer may consist of multiple materials. Moreover, there is nothing in the claim language itself or in the other intrinsic evidence stating, or even implying, that the glue layer must be comprised of only a single material. The Court also notes that Atmel has failed to set forth any argument in support of its contention that the term glue layer should be construed as "a layer of material of a single composition." See Defendant Atmel Corporation's Post-Hearing Submission Regarding Claim Construction ("Def.'s Post-Hearing Brief") at 7-9. In addition,

claim 1 states that "said glue layer *comprises* at least one member selected from the group consisting of conducting nitrides" '335 Patent at col. 6:4-6 (emphasis added), and both parties have jointly stipulated that the term "comprises" as it appears in the '335 patent means "includes at least the following but does not exclude others," Joint Statement of Claim Terms at 1. The Court concludes that the term glue layer should not be construed as being limited to consisting of only a single material.

As to how the term glue layer should be construed with respect to its adherence to other materials, Agere argues that the specification reveals that the patentee intended the term to have a particular meaning. The specification states: "A glue layer is a layer of material deposited prior to the tungsten and which has good adhesion both to the underlying dielectric layer and to the tungsten." '335 Patent at col. 2:30-33. Thus, the specification supports Atmel's construction with respect to adherence.

Atmel's sole argument in support of its contention that the glue layer must, in addition, adhere well to the exposed material at the bottom of the contact hole is based upon a statement made by the patent applicants during the prosecution history. After an initial rejection of claim 1 on July 20, 1987, a second rejection on February 20, 1988, and a third rejection on August 11, 1988, the patent applicants (in an Amendment After Final Rejection dated February 15, 1989) sought to amend claim 1 to add the following (after the words "CHARACTERIZED IN THAT"): "a portion of said glue layer overlies said exposed underlying material and said tungsten contacts said portion of said glue layer that overlies said underlying material and . . . ." Exhibit AG 006890 from 12/05/02 Hearing. Referring to this proposed amended language, the patent applicants attempted to overcome the previous rejections and distinguish their purported

invention from a prior art reference by contending that the prior art reference "does not state that the [glue layer] is deposited through a hole onto an underlying material (e.g. substrate) and, consequently, shows no appreciation for the requirement that the [glue layer] must adhere well to the substrate, as well as the dielectric." Exhibit AG 006891 from 12/05/02 Hearing. However, this effort to amend claim 1 in order to avoid the prior art was unsuccessful because the Patent and Trademark Office considered the Amendment After Final Rejection, determined that the proposed amendment was insufficient to overcome the previous rejections, concluded that the proposed amendment would raise new issues not related to the reasons for the previous rejections, and did not enter the amendment. See Exhibit AG 006899 from 12/05/02 Hearing. Thus, the proposed amendment was never added to claim 1 and the applicants' explanation for how this amended language would distinguish their invention from the prior art does not bear on our task, which is to construe the language of claim 1 as it appears in the final issued patent.

Accordingly, the Court construes "glue layer" to mean "a layer, composed of one or more materials, which is deposited prior to the tungsten and which has good adhesion both to the underlying dielectric layer and to the tungsten."

4. "covering"

Agere argues that the term "covering" should be construed as "lying or spreading over." Atmel argues that the term "covering" should be construed as "directly contacting from above." The Court concludes that neither construction is appropriate and therefore will provide its own construction of the term "covering."

The Court has referred to Webster's Third New International Dictionary, which provides a number of definitions for "cover." The definition which is clearly most relevant to the instant

context is: "to lie over: spread over: be placed on or often over the whole surface of." Webster's Third New International Dictionary of the English Language 524 (1986).[2] Employing this ordinary meaning of the term "covering" in claim 1 in its entirety would *allow for the possibility, but would not necessarily require,* that a glue layer "covering" a dielectric and an exposed underlying material would be in direct contact with both the dielectric and the exposed underlying material. Thus, it is not clear from the face of the claim language and the ordinary meaning of the claim language whether direct contact is required.

The specification provides some guidance as to whether direct contact is necessary. The specification states: "The glue layer film may be deposited, through openings in the dielectric, *directly on* the silicon or on a conducting material, such as a silicide, overlying the silicon. Of course, the glue layer is also deposited *on* the dielectric." '335 Patent at col. 3:7-11 (emphasis added). This language indicates that the patentee contemplated that the glue layer would be in direct contact with both the dielectric and the exposed underlying material, and indicates that one of ordinary skill in the art, reading the patent, would have so understood the term "covering."

Moreover, the prosecution history reveals that the patent applicants distinguished their invention from the prior art based on the requirement that there be direct contact between the glue layer and the exposed underlying material. The patent applicants distinguished their purported invention from a prior art reference by pointing to the language in claim 1 referring to the glue layer "covering said dielectric and said exposed underlying material," and asserting that the claim language "clearly recite[s] that the aluminum layer contacts not only the insulating layer but also the underlying material." Exhibit AG 006893 from 12/05/02 Hearing. The patent

[2] Notably, Agere has adopted this definition in part, but has omitted the language "be placed on."

applicants further asserted that in the prior art reference, which employed a thin aluminum layer to improve adhesion, "the aluminum layer touches only the insulating layer; it apparently does not contact the underlying silicon substrate." Exhibit AG 006896 from 12/05/02 Hearing.[3] The applicants argued that "such contact is clearly recited" in the applicants' own claim, rendering the applicants' claim "unobvious." Id. Thus, the patent applicants relinquished a construction of the term "covering" that would not require direct contact between the glue layer and both the dielectric and the exposed underlying material. See also Exhibit AG 006874 from 12/05/02 Hearing.

Accordingly, the term "covering" is construed as "lying over and directly contacting."

5. "said silicon surface"

Agere argues that the phrase "said silicon surface" in claim 2 should be construed as "a silicon surface." Atmel does not propose a construction of the phrase "said silicon surface," but rather contends that the phrase lacks an antecedent basis and is therefore indefinite and invalid. Because there is no actual dispute over the construction of the term "silicon surface," no construction is necessary at this time. Rather, the issue here is whether the term "silicon surface" is rendered indefinite and therefore invalid by the existence of the preceding word "said."

Atmel is certainly correct, and Agere appears to acknowledge, that the phrase "said silicon surface" lacks an antecedent basis (*i.e.*, there is no prior reference to a "silicon surface" in the claims). However, this does not necessarily render the phrase invalid for indefiniteness. The definiteness requirement arises out of 35 U.S.C. § 112, which requires that the "specification

[3] The Court notes that many of the prosecution history documents appear to have been numbered out of order.

shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2.

> Under 35 U.S.C. § 282 . . . , a patent is presumed valid, and at trial [the defendant has] the burden of proving facts by clear and convincing evidence showing that the patent is invalid. Compliance with the definiteness requirement is a question of law which we review *de novo*. Whether a claim is invalid for indefiniteness depends on whether those skilled in the art would understand the scope of the claim when the claim is read in light of the specification.

North American Vaccine, Inc. v. American Cyanamid Co., 7 F.3d 1571, 1579 (Fed. Cir. 1993) (citations omitted).

Here, when claim 2 is read in light of the specification, it is clear that "said silicon surface" means "a silicon surface." For example, the specification states: "We have found that tungsten can be blanket deposited with good adhesion over a dielectric covering a portion of a silicon surface . . . . The glue layer film may be deposited, through openings in the dielectric, directly on the silicon or on a conducting material, such as a silicide, overlying the silicon." '335 Patent at col. 3:3-10. Thus, the patentee expressly contemplated that the glue layer would be used both where the exposed underlying material beneath the dielectric is simply a silicon surface, and also where the exposed underlying material beneath the dielectric is a metallic silicide overlying a silicon surface. These two possible scenarios identified in the specification comport perfectly with the two scenarios addressed in claims 2 and 3, which assert "[a] method as recited in claim 1 in which said [exposed underlying] material comprises said silicon surface," and "[a] method as recited in claim 1 in which said [exposed underlying] material comprises a metallic silicide," respectively. '335 Patent at col. 6:7-10. Therefore, the Court concludes that

those skilled in the art would understand the scope of the claim when read in light of the specification, and thus Atmel's argument that the claim is invalid for indefiniteness is rejected.

6. "etching"

Agere argues that the term "etching" should be construed as "removing material through chemical reaction and/or physical action." Atmel presently argues that the term "etching" should be construed as "the process for removing material in a specified area through a wet or dry chemical reaction, or by physical removal, such as by sputter etch." The Court notes that Atmel's present proposed construction provides that "etching" can include removing material by physical action, see Def.'s Post-Hearing Brief at 9, whereas Atmel's proposed construction prior to the Markman hearing provided that etching only applied to removing material through chemical reaction and not through physical action, see Atmel Corporation's Claim Construction Brief Filed Pursuant to the Court's Order of October 18, 2002 ("Def.'s Second Brief") at 32. Prior to the Markman hearing, this was the only significant difference between the parties' proposed constructions. There now appears to be no significant difference between the proposed constructions. The Court finds that either construction would be acceptable, but concludes that Atmel's present proposed construction is slightly preferable as it appears to be precisely the definition provided in the treatise Microchip Fabrication, see Peter Van Zant, Microchip Fabrication 507 (2d ed. 1990), which treatise was relied upon as authoritative by Agere's expert witnesses, see Tr. 12/05/02 at 53-54. Accordingly, the Court construes the term "etching" as "the process for removing material in a specified area through a wet or dry chemical reaction, or by physical removal, such as by sputter etch."

7. "low pressure chemical vapor deposition"

The parties agree that the term "chemical vapor deposition" means "a process in which one or more gases chemically react with each other and/or with a surface material thereby producing a solid substance (such as tungsten)." See Joint Statement of Claim Terms at 2. Agere argues that the phrase "low pressure chemical vapor deposition" (or "LPCVD") should be construed as "chemical vapor deposition that is carried out at reduced pressure relative to atmospheric pressure." Atmel argues that the phrase "low pressure chemical vapor deposition" should be construed as "chemical vapor deposition that is carried out at pressures below approximately to 2 torr."

According to the expert testimony provided during the Markman hearing, chemical vapor deposition refers to a process in which a silicon wafer is placed in a reactor, certain gases are pumped into the reactor, and the gases react with each other (and may also react with the substrate) resulting in the deposition of a layer of tungsten on the substrate. See Tr. 12/05/02 at 55-56. It is also undisputed that the term "low pressure" preceding the term "chemical vapor deposition" describes the range of pressure inside the reactor at which the patentee intended the chemical vapor deposition to occur. The dispute here concerns the precise pressure range to which the term "low pressure" refers. Agere contends that "low pressure" means any pressure below atmospheric pressure (or 760 torr). Atmel, on the other hand, contends that the term "low pressure" refers to some smaller and more precise pressure range, although Atmel has been unable to settle on a precise proposed range.[4]

[4] In its initial Claim Construction Brief, Atmel argued that "low pressure" refers to a range between 0.5 and 1 torr. See Atmel Corporation's Opening Claim Construction Brief ("Def.'s Opening Brief") at 35. In its second Claim Construction Brief, Atmel argued that "low pressure" could refer to a range between 0.1 and 100 Militorr, or to a range between 0.25 and 2.0 torr, or to a range between 0.5 and 1 torr, emphasizing that "low pressure" refers to systems (continued...)

The Court must determine the ordinary and accustomed meaning of the technical phrase "low pressure chemical vapor deposition" as it would have been understood by one of ordinary skill in the art at the time of the invention. See Bell Atlantic, 262 F.3d at 1267. The '335 patent arises from a patent application originally filed in 1986. The only evidence offered by Agere to support its construction of "low pressure" is the definition set forth on a current website. See Exhibit A26-27 from 12/05/02 Hearing. Agere has not shown that such a definition would have been applicable at the time of the invention. Atmel, on the other hand, has offered a number of pertinent definitions from treatises. The first edition of the treatise Microchip Fabrication, printed in 1984, 1985 and 1986, states that "LPCVD systems operate in a pressure range from 0.1 Militorr – 100 Militorr." Peter Van Zant, Microchip Fabrication 181 (1st ed. 1986). The second edition, with a copyright date of 1990, provides that one particular LPCVD system (the "Horizontal conduction-convection-heated LPCVD") operates in "a pressure range of 0.25 to 2.0 torr." Peter Van Zant, Microchip Fabrication 309 (2d ed. 1990).

The evidence and expert testimony introduced by the parties clearly establishes that a person of ordinary skill in the art at the time of the invention would have understood the term

[4](...continued)
which operate "well below atmospheric pressure." Def.'s Second Brief at 33. At the Markman hearing, Atmel's expert witness explained that, practically speaking, low pressure chemical vapor deposition is not performed at pressure levels approaching atmospheric pressure because the deposition rate at such high pressure levels would be undesirably slow. See Tr. 12/05/02 at 222-23. Atmel's expert witness testified that the typical range for low pressure chemical vapor deposition "is somewhere around one torr," with pressures as high as "a few torr" and as low as "maybe .2 torr." Id. at 223. There is even a discrepancy between Atmel's present proposed construction of "low pressure" in its Revised Proposed Order Regarding Claim Construction ("chemical vapor deposition that is carried out at pressures below approximately to 2 torr") and its Post-Hearing Brief ("CVD at pressures below 1 torr"), see Def.'s Post-Hearing Brief at 10. In fact, even in its Post-Hearing Brief, Atmel "acknowledges that, because LPCVD is defined more often by example than explicitly, an upper limit of approximately 2 torr to 5 torr may be appropriate." Id.

"low pressure" to refer only to an *approximate* pressure range well below 760 torr, and not to any precise pressure range with specifically defined lower or upper limits. The evidence and expert testimony also indicates that at the time of the invention, low pressure chemical vapor deposition would typically have been carried out at pressures no higher than 2 or 3 torr. Thus, the Court construes "low pressure chemical vapor deposition" to mean "chemical vapor deposition that is carried out at pressures well below atmospheric pressure (760 torr), typically at pressures below approximately 2 or 3 torr."

V. CONSTRUCTION OF THE CLAIMS IN THE '672 PATENT

A. Background to the '672 Patent

Like the '335 patent, the '672 patent generally involves the formation of electrical interconnections using tungsten in a semiconductor device. However, the '672 patent addresses a particular problem encountered during tungsten deposition that is distinct from the adhesion problem addressed in the '335 patent.

Tungsten is often used to form electrical contacts with "device junctions." As the term is used in the '672 patent, device junctions are components (such as the source or drain regions of a transistor) that are located in the semiconductor substrate. Such junctions are either "N-type" (the charge carriers are negatively-charged particles) or "P-type" (the charge carriers are positively-charged particles) and, ordinarily, the junction type will be opposite to the type of substrate in which the junction sits (*i.e.*, N-type junctions will sit in P-type substrates, and P-type junctions will sit in N-type substrates). One problem encountered when forming tungsten contacts to such junctions is that, when the junction depth is shallow, certain chemicals introduced during tungsten deposition (referred to as "deposition precursors") such as tungsten

hexafluoride (WF_6) may react with, penetrate, and consume the junction material. Furthermore, the more shallow a device junction, the more easily the junction can be penetrated and consumed as a result of these undesirable reactions.

One approach to preventing such undesired reactions between deposition precursors and junction material involves the use of "barrier layers," which are layers of material that are deposited over junctions and which are intended to prevent interaction between deposition precursors and the junction material. Apparently, traditional barrier layers often fail to prevent such interactions entirely. The '672 patent asserts a method of depositing tungsten under controlled conditions whereby any undesirable reaction of tungsten precursors with the junction material is "self-limiting" so that any undesirable reaction ceases on its own before the thickness of the reaction product reaches the full junction depth. By combining this method with the use of a barrier layer, the '672 patent purportedly provides two measures of protection against damage to the junction material, thereby enabling the formation of reliable tungsten contacts in connection with shallow junctions. Claims 1-3 and claim 5 of the '672 patent are at issue in this lawsuit.

B. The '672 Claims

The '672 patent sets forth the following claims (with the disputed claim terms underlined):

> 1. A process for fabricating a semiconductor device comprising the steps of treating a substrate by forming a passage through a region overlying a device junction, depositing a material over at least a portion of said region to form an electrical contact to said junction together with an electrical conducting region and progressing towards completing said device, characterized in that said passage has an aspect ratio of at least 1.1, said junction has a depth shallower than

> 2500 [Angstroms], and said electrical contact and said conductive region on said surface comprises a deposition of 1) a material that presents a barrier to the solid-state diffusion of tungsten and 2) a deposition of tungsten by interaction of said substrate with a deposition comprising WF6 entities and a reducing agent wherein said substrate is heated to a deposition temperature in the range 250° C. to 600° C. during said tungsten deposition wherein said deposition temperature and environment is controlled such that said interaction is self-limiting with a self-limiting thickness less than said junction depth and wherein said deposition temperature is chosen such that the yield of said junctions decrease not more than 10% compared to the yield obtained for the same function having a via aspect ratio of .75 and having a contact of only aluminum.
>
> 2. The process of claim 1 wherein said reducing agent comprises hydrogen.
>
> 3. The process of claim 2 wherein said diffusion barrier comprises titanium nitride.
>
> 4. The process of claim 2 wherein said diffusion barrier comprises a titanium/tungsten alloy.
>
> 5. The process of claim 1 wherein said diffusion barrier comprises titanium nitride.
>
> 6. The process of claim 1 wherein said diffusion barrier comprises a titanium/tungsten alloy.

'672 Patent at col. 6:50 through col. 8:8.

Atmel generally contends that claim 1 as a whole is indefinite, and offers a number of arguments in support of this contention. In addition, the parties dispute the proper construction of the term "substrate" and the phrase "same function" in claim 1.[5] The Court will first construe the term "substrate" and the phrase "same function."

1. "substrate"

[5] Atmel also addresses the term "interaction" and the phrase "deposition comprising WF6 entities and a reducing agent" in its brief. However, Atmel does not propose constructions, but instead simply notes that its "contentions regarding the indefiniteness of these claim terms rests not on how they are themselves interpreted, but rather on the fact that the claim, regardless of how the words themselves are construed, is indefinite." Def.'s Post-Hearing Brief at 16-17.

Agere argues that the term "substrate" should be construed as "any material on which other materials may be formed or deposited." Atmel argues that the term "substrate" should be construed as "the underlying material upon which a device, circuit or epitaxial layer is fabricated." Atmel essentially contends that the term "substrate" applies only to the semiconductor wafer itself, whereas Agere wishes to construe the term more broadly. The Court concludes that the term should not be construed as referring only to the semiconductor wafer itself. However, because the Court finds Agere's construction to be unnecessarily broad, the Court shall provide its own construction of the term.

Claim 1 itself states that the first step of the process is "treating a substrate" and explains that this is accomplished by, first, "forming a passage through a region overlying a device junction," and second, "depositing a material over at least a portion of said region." '672 Patent at col. 6:50-54. The parties have agreed that "passage" as used in the '672 patent means "a hole that exposes a device junction," Joint Statement of Claim Terms at 4, and Atmel readily concedes that "a junction is essentially a region that has been created in the semiconductor substrate," Def.'s Second Brief at 43. It is also undisputed that this "region overlying a device junction" through which a passage is formed refers to a "dielectric layer positioned above the semiconductor substrate." Id.; see also '672 Patent at col. 1:29-32. Thus, since the claim 1 language itself expressly provides that the process of "treating a substrate" includes forming a passage through the dielectric layer above the semiconductor substrate, the "substrate" which is being treated must encompass both the semiconductor substrate and the dielectric region above it. Similarly, claim 1 also recites that tungsten is then deposited by a process in which "said substrate is heated to a deposition temperature in the range 250° C. to 600° C." '672 Patent at

col. 6:65-66. At this stage in the process, it is clear that both the dielectric and the barrier layers have already been deposited on the silicon wafer. Thus, the term "substrate" here clearly refers to more than the silicon wafer alone.

Moreover, an examination of the specification reveals that the patentee consistently used the term "silicon substrate" or "silicon prototype wafer" to refer to a bare silicon wafer with no additional layers of material, and the term "substrate" to refer to the entire entity comprising an underlying silicon wafer and any additional materials, such as a dielectric layer, deposited over the wafer. See '672 Patent at col. 2:45-53; col. 3:22-67; col. 5:44-48. Thus, a person of ordinary skill in the art would have understood the term "substrate" when used without the modifier "silicon" to mean "any underlying material or materials (such as a silicon wafer alone or a silicon wafer combined with other layers such as a dielectric layer) upon which other materials may be formed or deposited."

2. "same function"

Agere argues that the term "function" as used in the '672 patent would be interpreted by a person of ordinary skill in the art as a misspelling of the term "junction." Atmel argues that the term "function" as used in the '672 patent should be construed as "purpose." Despite Atmel's contention, both parties' expert witnesses testified that the phrase "same function" means "same junction" (*i.e.*, a junction having a depth shallower than 2500 Angstroms). See Tr. 12/05/02 at 76, 227-28. In addition, the specification includes a clause that is nearly identical to the clause in claim 1 (in which the disputed term "function" appears) except that the word "junction" is used in place of the word "function" in the specification. See '672 Patent at col. 4:32-37 ("The temperature should preferably be chosen such that the device yield of working test junctions

decreases no more than 10% compared to the yield obtained for the same *junction* having a via aspect ratio of 0.75 and with a contact of only aluminum." (emphasis added)). Where claim language is ambiguous on its face, the remaining intrinsic evidence, including the specification, is properly examined to resolve such ambiguity. See Interactive Gift Express, 256 F.3d at 1331.

Despite the fact that its own expert witness was persuaded that the term "function" is simply a misspelling of the term "junction," and despite the fact that the intrinsic evidence supports such a conclusion, Atmel continues to take the position that the term is not a misspelling and that it should be construed in accordance with the ordinary meaning of the term "function." The Court finds Atmel's position untenable and rejects its proposed construction. Accordingly, the term "function" is construed as a misspelling of the term "junction."

Atmel also contends that even if the Court construes the term "function" as a misspelling of "junction," the meaning of the phrase "same junction" is vague and indefinite when considered in light of the surrounding claim language and the information in the specification. See Def.'s Post-Hearing Brief at 21-22. However, Atmel's own expert acknowledged on cross-examination that the phrase "same [j]unction" refers to the kind of junction previously recited in the claim, namely a "device junction" that "has a depth shallower than 2500 [Angstroms]." See Tr. 12/5/02 at 261. Thus, Atmel's contention that the meaning of the phrase "same [j]unction" is unclear is rejected.[6]

[6] Atmel has not offered a proposed construction of the phrase "same [j]unction," and therefore the Court need not construe the phrase but need only resolve Atmel's argument that the phrase is unclear and causes the claim to be indefinite.

3. "wherein said deposition temperature and environment is controlled such that said interaction is self-limiting with a self-limiting thickness less than said junction depth"

Atmel contends that this passage, containing over twenty individual terms, should be construed as a single phrase. See Def.'s Second Brief at 48. Initially, the Court notes that the parties do not cite any case law to support the implicit proposition that it is appropriate for a Court under certain circumstances to provide a construction for a passage in the claims which contains such a large number of individual terms, nor do the parties provide any reasons why, even if permissible, the Court should construe this passage as a single phrase.

At the crux of Atmel's arguments regarding this phrase are two specific contentions. The first actually goes to what Atmel contends should be the construction of the individual terms "self-limiting" and "self-limiting thickness." Atmel contends that such terms would have had no independent meaning to a person of ordinary skill in the art. See Def.'s Second Brief at 48. Furthermore, Atmel contends that the patentee chose to be his own lexicographer and to provide clear definitions for these terms in the specification. See Def.'s Post-Hearing Brief at 19. The Court agrees. The specification states:

> The self-limiting effect is characterized by a tungsten formation rate at 10 minutes that is less than 10% of the initial equilibrium rate. The self-limiting thickness is the tungsten thickness under these conditions achieved at 10 minutes.

'672 Patent at col. 3:68 through col. 4:4. Even Agere's expert witness acknowledged that this language provides clear definitions for the terms "self-limiting effect" and "self-limiting thickness." See Tr. 12/5/02 at 152-54. Thus, the Court construes "self-limiting" as "exhibiting an effect that is characterized by a tungsten formation rate at 10 minutes that is less than 10% of

the initial equilibrium rate."[7] The Court further construes "self-limiting thickness" as "the tungsten thickness achieved at 10 minutes under conditions in which a 'self-limiting effect' is achieved, *i.e.*, the tungsten formation rate at 10 minutes is less than 10% of the initial equilibrium rate."

However, Atmel goes even further, arguing that the claim language in question should be construed as not covering the use of an environment that includes a cold wall reactor in the temperature range of 250 to 600 degrees C. See Def.'s Post-Hearing Brief at 19-20. Atmel apparently contends that this limitation should be read into the claim language in question as a result of the language appearing in the specification immediately before and after the above-quoted language defining "self-limiting effect" and "self-limiting thickness":

> Conditions should be chosen such that a self-limiting effect with a self-limiting thickness smaller than the junction thickness is achieved on the silicon prototype wafer in the 250° C. to 600° C. temperature range. (The self-limiting effect is characterized by a tungsten formation rate at 10 minutes that is less than 10% of the initial equilibrium rate. The self-limiting thickness is the tungsten thickness under these conditions achieved at 10 minutes.) For example, when a hot wall, e.g., tube reactor . . . is employed with tungsten hexafluoride and argon, the self-limiting thickness vs. temperature is shown in FIG. 1. Similarly, when a cold wall reactor . . . is utilized in the temperature range 250° C. to 600° C. no self-limiting effect is observed and thus under these conditions this reactor should not be employed.

'672 Patent at col. 3:64 through col. 4:13. However, the specification language pertaining to the unsuccessful use of a cold wall reactor in the temperature range of 250 to 600 degrees C. simply does not appear in the claim language, nor can this purported limitation be understood as being part of a definition of a specific term or phrase in the claim language. Rather, the specification

[7] It should be noted that there is apparently no dispute that "equilibrium rate" means the initial tungsten formation rate. See Tr. 12/5/02 at 154.

language indicating that a self-limiting effect is not observed using a cold wall reactor in the temperature range of 250 to 600 degrees C. appears to present merely an illustration of conditions that may not produce the desired result. Thus, it would be improper to read this purported limitation from the specification into the claims. See Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186 (Fed. Cir. 1998).

Atmel's second contention with regard to the claim language in question is that 35 U.S.C. § 112, ¶ 6 applies to claim 1, and that, because claim 1 does not satisfy the requirements set forth in 35 U.S.C. § 112, ¶ 6, claim 1 is invalid for indefiniteness. Section 112, ¶ 6 provides:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. § 112, ¶ 6. The word "combination" in this paragraph can include a combination of mechanical elements in an apparatus claim, a combination of substances in a composition claim, or a combination of steps in a method or process claim. See O.I. Corp. v. Tekmar Co., Inc., 115 F.3d 1576, 1582-83 (Fed. Cir. 1997). In combination *apparatus* claims, a patent applicant can claim a specified function without reciting in the claim itself the *structures* or *materials* necessary for performing that function. See id.; Apex Inc. v. Raritan Computer, Inc., 2003 WL 1725618, at *5 (Fed. Cir. 2003). Such claim limitations are referred to as "means-plus-function" limitations. See Apex Inc., 2003 WL 1725618, at *5. Similarly, in combination *method* or *process* claims, a patent applicant can claim a specified function without reciting in the claim itself the *acts* necessary for performing that function. See O.I. Corp.,115 F.3d at 1583. Such claim limitations are referred to as "step-plus-function" limitations. Apex Inc., 2003 WL

1725618, at *5. Moreover, when an applicant takes advantage of the convenience of employing a "means-plus-function" or "step-plus-function" limitation, such claim is limited to the means or steps specified in the written description, and equivalents thereof. O.I. Corp., 115 F.3d at 1583.

A threshold question is whether § 112, ¶ 6 applies to a particular limitation. Here, there is no dispute that claim 1 is a process claim. In method or process claims, § 112, ¶ 6 "is implicated only when steps plus function without acts are present," *i.e.*, when "an element in a combination method or process claim [is] recited as a step for performing a specified function without the recital of acts in support of the function." O.I. Corp., 115 F.3d at 1583.

> Therefore, when the claim language includes sufficient acts for performing the recited function, § 112, ¶ 6 does not apply. Again similar to a means-plus-function analysis, the absence of the phrase "step for" from the language of a claim tends to show that the claim element is not in step-plus-function form. However, claim elements without express step-plus-function language may nevertheless fall within § 112, ¶ 6 if they merely claim the underlying function without recitation of acts for performing that function. Unfortunately, method claim elements often recite phrases susceptible to interpretation as either a function or as an act for performing a function. Both acts and functions are often stated using verbs ending in "ing." . . . In such circumstances, claim interpretation requires careful analysis of the limitation in the context of the overall claim and the specification.
>
> In general terms, the "underlying function" of a method claim element corresponds to what that element ultimately accomplishes in relationship to what the other elements of the claim and the claim as a whole accomplish. "Acts," on the other hand, correspond to how the function is accomplished. Therefore, claim interpretation focuses on what the claim limitation accomplishes, i.e., it's underlying function, in relation to what is accomplished by the other limitations and the claim as a whole. If a claim element recites only an underlying function without acts for performing it, then § 112, ¶ 6 applies even without express step-plus-function language.

Seal-Flex, Inc. v. Athletic Track and Court Const., 172 F.3d 836, 849-50 (Fed. Cir. 1999) (J. Rader, concurring).

The Court has considered the threshold issue of whether § 112, ¶ 6 applies to the claim language in question. As stated above, the issue here is whether the language in this combination process claim sets forth an element that is recited as a step for performing a specified function without the recital of acts in support of the function. Atmel argues that the language in question ("wherein said deposition temperature and environment is controlled such that")

> contains no guidance as to how the deposition temperature and environment are to be controlled to achieve the self-limiting effect and thickness . . . . Therefore, despite the absence of 'step for' language, the limitation should be treated under § 112, ¶ 6 and construed to cover only the corresponding steps in the specification, and equivalents thereof, for achieving the self-limiting effect and thickness.

Def.'s Post-Hearing Brief at 19. In response to this argument, Agere contends simply that, "because the claim language clearly recites an act – i.e., controlling the temperature and environment – Atmel's 'step-plus-function' argument fails." Pl.'s Post-Hearing Brief at 24. Agere also notes that "[c]ourts have been extremely reluctant to interpret process claims as employing 'step-plus-function' limitations," citing to Seal-Flex, 172 F.3d at 850 n.5 (Rader, J., concurring). Atmel counters: "The claim implicates § 112, ¶ 6 because the claim does not teach how to achieve the desired outcome by specifying the act; the teaching appears, if at all, only in the specification." Def.'s Post-Hearing Brief at 19 n.12.

The Court agrees with Atmel that § 112, ¶ 6 applies to the claim language in question. During the Markman hearing, the following colloquy transpired between counsel for Atmel and Agere's expert witness:

> Q Going back to the claim limitation it says "wherein said deposition temperature and environment is controlled." The claim language doesn't tell you how it controlled the

temperature and the environment such that you achieve a self-limiting interaction with a self-limiting thickness less than said junction depth, does it?

A Your question is the claim language does not tell me how to control?

Q Right.

A It tells me that I need to use that temperature and that environment such that the following occurs.

Q What does it tell you, the claim language, about how you control the environment?

A It just simply says that I have to use whatever environment and deposition temperature such that the interaction and so forth occurs.

Q But the claim language doesn't tell you what you're supposed to do to manipulate or vary the deposition temperature in the environment such that you achieve the interaction that is self-limiting with a self-limiting thickness, does it?

A The specification does describe how one would go about or how the inventor suggests one goes about as to obtain those results.

Q So you need to go to the specification to determine how you achieve the result that the interaction is self-limiting with a self-limiting thickness less than said junction depth, correct?

A That's not exactly what I said. I said the specification describes how one finds when interaction would be self-limiting or not. So one can use that to identify how to choose a temperature and environment such that that interaction occurs.

Tr. 12/5/02 at 156-58. Thus, as acknowledged by Agere's own expert witness, and as asserted by Atmel's expert witness, see Tr. 12/5/02 at 225-26, it is only in the specification of the '672 patent that one reading the patent would find the information necessary to allow one to determine the "deposition temperature and environment" that should be used to achieve the desired function. See '672 Patent at col. 3:56 through col. 4:21. Therefore, the Court concludes that although the claim language in question does not include express step-plus-function language, the claim language nevertheless falls within § 112, ¶ 6 because it recites a step (controlling the deposition

temperature and environment) for performing a specified function ("such that said interaction is self-limiting with a self-limiting thickness less than said junction depth") without reciting the acts necessary to perform this step and achieve this function.

Once it is determined that a claim includes a step-plus-function limitation, the Court must then construe the limitation "to cover the corresponding . . . acts described in the specification." 35 U.S.C. § 112, ¶ 6; Chiuminatta Concrete Concepts, Inc. v. Cardinal Industries, Inc., 145 F.3d 1303, 1308 (Fed. Cir. 1998). In other words, this Court must now turn to the written description of the patent to find the acts that correspond to the step in claim 1 requiring that the deposition temperature and environment be controlled "such that said interaction is self-limiting with a self-limiting thickness less than said junction depth." B. Braun Medical, Inc. v. Abbott Laboratories, 124 F.3d 1419, 1424 (Fed. Cir. 1997).

The Court concludes that the acts in the specification corresponding to this limitation are set forth in the following passage:

> The precise conditions suitable for the tungsten deposition vary with reactor design. Appropriate conditions are determined by performing a control sample in the desired deposition apparatus utilizing 1) a precursor composition including only tungsten hexafluoride and argon and 2) a bare silicon prototype wafer that has been subjected to an implant dose equivalent to the total implant does that is ultimately to be employed in the device. Conditions should be chosen such that a self-limiting effect with a self-limiting thickness smaller than the junction thickness is achieved on the silicon prototype wafer in the 250˚ C. to 600˚ C. temperature range.

'672 Patent at col. 3:56-67. However, the Court does not agree with Atmel that the next passage, referring to the use of hot wall and cold wall reactors, should be included in construing the step-plus-function limitation, since this passage appears to set forth merely illustrative examples and

not required limitations. See '672 Patent at Col. 4:4-13 ("For example, when a hot wall reactor . . . is employed with tungsten hexafluoride and argon, the self-limiting thickness vs. temperature is shown in FIG. 1. Similarly, when a cold wall reactor . . . is utilized in the temperature range 250° C. to 600° C. no self-limiting effect is observed and thus under these conditions this reactor should not be employed.").

In sum, the Court construes "self-limiting" as "exhibiting an effect that is characterized by a tungsten formation rate at 10 minutes that is less than 10% of the initial equilibrium rate." The Court further construes "self-limiting thickness" as "the tungsten thickness achieved at 10 minutes under conditions in which a 'self-limiting effect' is achieved, *i.e.*, the tungsten formation rate at 10 minutes is less than 10% of the initial equilibrium rate." The Court also concludes that the claim language in question recites a step-plus-function limitation, and that this limitation should be construed in accordance with the specification language quoted above, see '672 Patent at col. 3:56-67.

4. "wherein said deposition temperature is chosen such that the yield of said junctions decrease not more than 10% compared to the yield obtained for the same [j]unction having a via aspect ratio of .75 and having a contact of only aluminum"

The Court has carefully reviewed the two arguments raised regarding the claim language above, and has concluded that additional clarification by the parties will be required before the Court is able to address and resolve these arguments. These two issues are: (1) whether the term "yield" is inadequately defined in the patent, thereby rendering claim 1 indefinite, see Pl.'s Post-Hearing Brief at 25-26; Def.'s Post-Hearing Brief at 22; and (2) whether this claim language

includes a "step-plus-function" limitation, and therefore falls within § 112, ¶ 6, see Pl.'s Post-Hearing Brief at 27; Def.'s Post-Hearing Brief at 20-22.[8]

The Court has labored to comprehend the expert witness testimony presented at the Markman hearing regarding the meaning of the term "yield," but has found the testimony to be unenlightening at best. See, e.g., Tr. 12/5/02 at 79, 111-13, 161-67, 230-34. As to the "step-plus-function" issue, neither the scant testimony addressing this issue at the Markman hearing, nor the parties' discussions of the issue, provide meaningful assistance. Therefore, as set forth in the Supplemental Order following this Memorandum, the Court shall permit Atmel, if it wishes to further pursue these arguments, to file an additional brief addressing only these issues, and shall permit Agere to file a responsive brief. The parties may attach affidavits from their expert witnesses if the parties determine that additional expert witness testimony would assist the Court in resolving these two issues.

[8] As a corollary matter, if the claim includes a "step-plus-function" limitation, the Court would have to construe the limitation "to cover the corresponding . . . acts described in the specification." 35 U.S.C. § 112, ¶ 6; Chiuminatta Concrete Concepts, 145 F.3d at 1308.

VI. CONSTRUCTION OF THE CLAIMS IN THE '827 PATENT

A. Background to the '827 Patent

The '827 patent discloses methods for forming electrical contact structures in semiconductor integrated devices and addresses two particular problems that can occur during the fabrication of such devices. A layer of silicide is often formed on the surface of a semiconductor substrate, at least in those regions (such as source and drain regions) where a contact will eventually be required. The purpose of such a silicide layer is to minimize contact resistance, and to improve the electrical connection between the underlying junction and the metal that is formed in an opening in the dielectric layer above the substrate surface. The first problem addressed by the '827 patent is the potential loss of silicide material that can occur when an opening is etched into a dielectric layer to expose a contact region. The '827 patent discloses a method in which, after an opening is etched into the dielectric layer, a silicide-forming material is deposited into the opening, the wafer is heated in a non-oxidizing atmosphere, a reaction occurs between the silicide-forming material and the semiconductor substrate, and additional silicide material is formed to replenish any silicide consumed by the etching process.

The second problem addressed by the '827 patent occurs when the openings etched into the dielectric layer are misaligned with the underlying contact region such that only a portion of the contact region is exposed. The '827 patent discloses a method in which dopants, such as phosphorous ions, are implanted into the contact region to correct for any such misalignment by extending the contact region in a lateral direction.

Claims 1-5 and 9-12 of the '827 patent are at issue in this lawsuit.

B. The '827 Claims

The ‘827 patent sets forth the following claims (with the disputed claim terms underlined):

> 1. In the manufacture of semiconductor integrated-circuit devices, a method for making electrical contact to at least one contact region on a semiconductor body, said method comprising the steps of
>
> depositing a dielectric layer on said body,
>
> etching an opening into said dielectric layer, said opening exposing an area which comprises at least a portion of said contact region, said contact region comprising a silicide formed before said etching step,
>
> implanting phosphorous after depositing said dielectric layer and etching said opening,
>
> depositing silicide-forming material after etching and implanting,
>
> heating in a non-oxidizing atmosphere, and
>
> depositing a metal layer.
>
> 2. The method of claim 1 in which said contact region comprises titanium silicide.
>
> 3. The method of claim 1 in which said silicide-forming material comprises titanium.
>
> 4. The method of claim 1 in which said atmosphere comprises a constituent which promotes formation of a conductive compound with said silicide-forming material.
>
> 5. The method of claim 4 in which said silicide-forming material comprises titanium, and in which said atmosphere comprises nitrogen.
>
> 6. The method of claim 5 in which said layer of silicide-forming material consists essentially of titanium and has a thickness in the range from 10 to 100 nanometers, and in which heating is at a temperature in the range from 750 to 950 degrees C. and for a duration in the range from 10 seconds to 1 minute, lower temperatures corresponding to longer times and conversely.
>
> 7. The method of claim 1, said contact being in a CMOS structure, and the dose of phosphorous implantation being less than or equal to 10 14/cm2.
>
> 8. The method of claim 1 in which said openings have a width which is less than or equal to 1 micrometer.
>
> 9. A method of manufacturing an integrated circuit comprising the steps of:
>
> forming an electrical contact region on a semiconductor body, said region comprising a silicide;

depositing, after said forming, a dielectric layer on said body and said contact region;

etching an opening into said dielectric layer, said opening exposing an area which comprises at least a portion of silicide of said contact region;

depositing a silicide-forming material after said etching;

heating in a non-oxidizing atmosphere; and

depositing a metal layer.

10. A method as recited in claim 9 in which said contact regions comprise titanium silicide.

11. A method as recited in claim 9 in which said silicide forming material comprises titanium.

12. A method as recited in claim 9 in which said atmosphere comprises a constituent which promotes formation of a conductive compound with said silicide forming material.

'827 Patent at col. 4:45 through col. 6:19.

1. "contact region" (and "electrical contact region"), "semiconductor body" and "opening"

The parties dispute the proper construction of the terms "contact region," (and "electrical contact region"),[9] "semiconductor body," and "opening." As the terms are set forth in the claims, and as evidenced by the parties' arguments regarding the proper construction of these terms, there is a strong interrelationship between them, and therefore the Court considers it appropriate to construe these terms simultaneously.

Agere argues: (1) that the term "contact region" means "an electrically conducting space or area to which another electrical conductor may be connected so as to allow current to pass"; (2) that the term "semiconductor body" means "any semiconductor material"; and (3) that the term "opening" means "a hole or void; an open space." Atmel argues: (1) that the term "contact

[9] The parties have stipulated that the term "contact region" and the term "electrical contact region" should be construed identically. See Def.'s Post-Hearing Brief at 14 n.9; Plaintiff's Post-Hearing Claim Construction Brief ("Pl.'s Post-Hearing Brief") at 31. For convenience, the Court will refer to both terms as "contact region."

region" means "a region of the semiconductor substrate to which electrical contact is made"; (2) that the term "semiconductor body" means "the underlying material upon which a device, circuit or epitaxial layer is fabricated" (*i.e.*, the substrate or the silicon wafer); and (3) that the term "opening" means "a contact hole, that is, [a hole] in the first dielectric layer that expose[s] the silicon surface (*i.e.*, the silicon substrate) or the conducting material at the silicon surface." The essential difference between the parties' constructions is that Atmel apparently wishes to construe the claim terms such that the claims cover only openings above *contact regions which are contained within the substrate or the silicon wafer*, whereas Agere wishes to construe the claim terms such that the claims cover openings above *contact regions which are formed in or on any semiconductor material*, including but not limited to the substrate or silicon wafer.

Agere's proposed constructions more closely comport with the general and ordinary meaning of these terms. For example, Agere provides a dictionary definition of the term "contact," which provides, in pertinent part: "the junction or touching surface of two electrical conductors through which a current passes." Webster's Third New Int'l Dictionary 490 (1986). Also, Agere provides a dictionary definition of "opening," which provides, in pertinent part: "an unobstructed or unoccupied space or place . . . a void in solid matter: a gap, hole, or aperture." Random House Dictionary of the English Language 1357 (2d ed. 1987).

Moreover, the specification indicates that Atmel's proposed constructions are too narrow. The "Background of the Invention" provides:

> Making electrical contact to semiconductor regions such as, e.g., source, drain, and gate regions of a field-effect transistor typically involves the deposition of a metallization over a dielectric which has been patterned to produce openings (windows, holes, vias) to the underlying semiconductor structure.

'827 Patent at col. 1:14-19. In addition, the "Detailed Description" of the specification provides:

> Contact openings may be, e.g., to source or drain regions of field-effect transistors, or to contact regions intended for device interconnections. Typically, in the latter case, contact is made to silicon in polycrystalline form.

'827 Patent at col. 2:30-34. According to the explanation provided by Agere's expert witness, this language makes clear that the patentee contemplated using the patented process not only for contact regions which are contained within the silicon substrate (such as source and drain regions), but also for contact regions which are not contained within the silicon substrate (such as gate regions). See Tr. 12/5/02 at 94-99. Thus, Atmel's proposed construction of "contact region" as "a region of the semiconductor substrate" is too narrow, as the contact region need not be contained within the substrate.

In addition, the patent does not provide that openings must be in the first dielectric layer and must expose the silicon substrate or wafer, but only that openings must expose an "underlying semicondcutor *structure*." '827 Patent at col. 1:18-19 (emphasis added). The patentee's decision to use the term "semiconductor structure" in the specification and the term "semiconductor body" in the claims, and not to use the term "semiconductor substrate" in either the specification or the claims, indicates a specific intention not to limit the claimed process to openings that are formed in the first dielectric layer above the silicon substrate.

Accordingly: (1) the term "contact region" is construed as "an electrically conducting space or area to which another electrical conductor may be connected so as to allow current to pass"; (2) the term "semiconductor body" is construed as "any semiconductor material"; and (3) the term "opening" is construed as "a hole, void, or open space."

2. Sequence of the steps of "heating in a non-oxidizing atmosphere" and "depositing a metal layer"

The parties do not dispute the meaning of these two phrases, but rather disagree as to whether the patent requires that the steps be performed in a particular sequence. Agere argues that the step of "heating in a non-oxidizing atmosphere" must be performed before the step of "depositing a metal layer." Atmel argues that it is not required that these two steps be performed in this order, and that one would be performing the process asserted in the '827 patent even if these two steps were performed in reverse order. The Court concludes that the '827 patent does not require that these two steps be performed in the order in which they are set forth in the claims.

"Unless the steps of a method actually recite an order, the steps are not ordinarily construed to require one." Interactive Gift Express, Inc. v. Compuserve, Inc., et al., 231 F.3d 859, 875 (Fed. Cir. 2000). An order may be imposed, however, if the substance of the claim language indicates that an order is logically required, see Mantech Environmental Corporation v. Hudson Environmental Services, Inc., 152 F.3d 1368, 1376 (Fed. Cir. 1998), or where such a sequential order is implicit from a review of the claim, the specification and the prosecution history, Loral Fairchild Corp. v. Sony Corp., 181 F.3d 1313, 1322 (Fed. Cir. 1999).

To begin with, there is nothing in the claim language itself which expressly requires, or even implicitly requires as a matter of logic, that the steps be performed in a particular order. Agere points to the fact that its expert witness testified at the Markman hearing that the preferred embodiment described in the '827 patent would not work if the order of the steps as set forth in the claims were reversed. This is because the preferred embodiment employs aluminum for the

metal layer, which has a melting temperature of approximately 500 degrees C., and employs a heating range of range of 750 to 950 degrees C. See Tr. 12/5/02 at 106-07. Thus, as to the preferred embodiment, if the aluminum were deposited first, it would subsequently melt during the heating in a non-oxidizing atmosphere. However, on cross-examination, Agere's expert witness conceded that the patent expressly allows for the use of other metals that might have higher melting points, in which case one could successfully practice the claimed invention with the sequence of the two steps reversed. See id. at 113-114. As there is no intrinsic evidence indicating that the two steps in question must always be performed in a certain sequence, the Court construes the claims not to require a particular sequence with regard to these two steps.

VII. CONSTRUCTION OF THE CLAIMS IN THE '126 PATENT

The parties initially disputed the proper construction of the term "overlying" and the phrase "additional material layer" as used in the '126 patent. However, Atmel did not offer any expert testimony or evidence regarding the '126 patent at the Markman hearing. Furthermore, in its post-hearing brief and proposed order, Atmel has not offered any proposed constructions or any arguments regarding any of the claim terms in the '126 patent. See Def.'s Post-Hearing Brief. Therefore, as there no longer appears to be any dispute over the proper construction of the term "overlying" and the phrase "additional material layer," the Court finds it unnecessary to construe these terms.

VIII. CONSTRUCTION OF THE CLAIMS IN THE '269 PATENT

A. Background of the '269 Patent

After a semiconductor chip is fabricated, it is usually mounted on what is called a "lead frame" (frequently a thin, copper frame) and then encapsulated in a "package" (often made of a

ceramic or plastic material). The package is intended to protect the chip from damage, and to provide a convenient way to make electrical connections to the circuitry of the chip.

The package contemplated by the '269 patent includes a surface called a "paddle," which is connected to an "external mounting frame" by "paddle support arms," and upon which a semiconductor chip is mounted. When the paddle is pressed down in the process of mounting the chip, deformation in the paddle support arms can occur. The '269 patent claims the invention of a structure that its inventors called a "deformation absorbing member" which exists as part of the paddle support arms. The purpose of the deformation absorbing members is to minimize the deformation that can occur when the paddle is pressed down.

Claims 1, 4, 6 and 9 of the '269 patent are at issue in this lawsuit.

B. The '269 Claims

The '269 patent sets forth the following claims (with the disputed claim terms underlined):

> 1. A semiconductor integrated circuit package comprising: a semiconductor integrated circuit chip; a lead frame, said lead frame having a paddle on which said chip is mounted and paddle support arms; and an external mounting frame having a plurality of fingers, electrical connections from said chip to said fingers, said paddle being connected to said external mounting frame by said paddle support arms CHARACTERIZED IN THAT said paddle support arms comprise a deformation absorbing member, said paddle being depressed with respect to said external mounting frame, said deformation absorbing member localizing deformation during paddle downsetting and maintaining desired physical characteristics.
>
> 2. A package as recited in claim 1 in which said deformation absorbing member comprises a T bar.
>
> 3. A package as recited in claim 1 in which said deformation absorbing member comprises an S bend member.
>
> 4. A package as recited in claim 1 in which said deformation absorbing member comprises an annular member.

5. A package as recited in claim 1 in which said deformation absorbing member comprises a wrinkle member.

6. A semiconductor integrated circuit package comprising:
a semiconductor integrated circuit chip;
a paddle on which said chip is mounted;
a plurality of paddle support arms, said paddle being connected to said paddle support arms;
a plurality of fingers;
electrical connections from said chip to said fingers;
CHARACTERIZED IN THAT said paddle support arms comprise a deformation absorbing member, said paddle being depressed with respect to at least a portion of said fingers, said deformation absorbing member localizing deformation during paddle downsetting and maintaining desired physical characteristics.

7. A semiconductor integrated circuit package as recited in claim 6 in which deformation absorbing member comprises a T bar.

8. A semiconductor integrated circuit package as recited in claim 6 in which deformation absorbing member comprises an S bend member.

9. A semiconductor integrated circuit package as recited in claim 6 in which deformation absorbing member comprises an annular member.

10. A semiconductor integrated circuit package as recited in claim 6 in which deformation absorbing member comprises a wrinkle member.

'269 Patent at col. 3:29 through col. 4:39.

1. "semiconductor integrated circuit package"

Agere argues that the term "semiconductor integrated circuit package" need not be construed because it appears only in the "preamble" and therefore does not constitute a claim limitation. In the alternative, Agere argues that the term means "a structure that allows a semiconductor integrated circuit chip to be mounted physically and contacted electrically." Atmel does not set forth an argument as to whether the term constitutes a claim limitation requiring construction. Atmel argues that the term "semiconductor integrated circuit package"

means "a structure in which the integrated circuit chip is mounted and encapsulated and which contains the means necessary for electrical interconnection of the chip to external components."

"A patent claim generally consists of three elements: a preamble, a transitional phrase -- such as 'comprising' -- and a body which contains the various elements and limitations of the structure, combination or method." Michaels v. Art Betterley Enterprises, Inc., 1995 WL 737925, at *7 (W.D.N.Y. 1995). Here, the language "A semiconductor integrated circuit package," appearing at the outset of claim 1 prior to the transitional phrase "comprising," constitutes the preamble. The threshold issue is whether this preamble constitutes a claim limitation, because when the preamble does not constitute a claim limitation, it need not be construed. See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 807-08 (Fed. Cir. 2002).

> Whether to treat a preamble as a limitation is a determination "resolved only on review of the entire[ ] . . . patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim." In general, a preamble limits the invention if it recites essential structure or steps, or if it is "necessary to give life, meaning, and vitality' to the claim." Conversely, a preamble is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention."

Id. at 808 (citations omitted). Except in cases in which the patentee clearly relied on the preamble during prosecution to distinguish the claimed invention from the prior art, "a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention." Id. at 808-09.

For example, in IMS Tech., Inc. v. Haas Automation, Inc., 206 F.3d 1422 (Fed. Cir. 2000), claim 1 of the patent began with the following preamble: "A programmable microcomputer control apparatus for controlling the relative motion between a tool and a workpiece comprising: . . . ." The Court held that the phrase "control apparatus" in the preamble "merely [gave] a descriptive name to the set of limitations in the body of the claim that completely set forth the invention," and that it did not constitute a claim limitation. Id. at 1434.

Similarly, the preamble language in claim 1 of the '269 patent ("A semiconductor integrated circuit package") need not be construed because it does not constitute a claim limitation. The claim body describes a structurally complete invention, and the deletion of the preamble phrase would not affect the structure of the claimed invention. The Court therefore concludes that this phrase need not be construed.

2. "lead frame," "external mounting frame," "paddle," "paddle support arms," and "fingers"

These five terms shall be construed together because their constructions are, to a significant extent, interrelated. The parties have jointly offered the following three proposed constructions: "lead frame" means "a frame upon which a semiconductor integrated circuit chip can be mounted that includes a paddle, a plurality of fingers, and a plurality of paddle support arms"; "paddle support arms" means "arms that support a paddle"; and "fingers" means "projecting pieces of a lead frame that are initially connected to the external mounting frame and that extend inward toward the center of the lead frame to facilitate electrical connections with a semiconductor integrated circuit chip." The constructions of the terms "external mounting frame" and "paddle" are disputed. Agere argues that the term "paddle" as used in the '269 patent

should be construed as "a surface for mounting a semiconductor integrated circuit chip." Atmel argues that the term "paddle" as used in the '672 patent should be construed as "a flat surface at the center of the lead frame on which the semiconductor integrated circuit chip is mounted." The essential difference between the parties' proposed constructions is that Atmel wishes to construe "paddle" to include some reference to its relationship to a lead frame, while Agere argues that no such reference in the construction is necessary. Finally, Agere argues that the term "external mounting frame" should be construed as "that portion of the lead frame that has a plurality of fingers and which is connected to the paddle by paddle support arms," while Atmel argues that the term should be construed as "the exterior portion of the lead frame to which the paddle support arms and fingers are attached before they are severed."

Looking only at the claim language itself for an understanding of these five terms, it would initially appear: (1) that a lead frame comprises (a) a paddle, and (b) paddle support arms; (2) that the lead frame is a separate conceptual entity from, and is connected to, the external mounting frame; and (3) that the external mounting frame comprises (a) fingers, and (b) electrical connections between the chip and the fingers. See '269 Patent at col. 3:29-36 ("A semiconductor integrated circuit package comprising: a semiconductor integrated circuit chip; a lead frame, said lead frame having a paddle on which said chip is mounted and paddle support arms; and an external mounting frame having a plurality of fingers, electrical connections from said chip to said fingers, said paddle being connected to said external mounting frame by said paddle support arms . . . ."). However, a careful reading of the specification reveals that the patentee implicitly, if not expressly, defined these terms in the following specific fashion. See Vitronics Corp., 90 F.3d at 1582 (citing Markman, 52 F.3d at 979).

According to the specification, a "lead frame" comprises not only the paddle and the support arms, but also the fingers and the external mounting frame as well. In other words, the "lead frame" comprises the entire single flat metal piece to which a chip is initially mounted. See '269 Patent at col. 1:24-25 ("The chip itself is mounted on a lead frame which has a plurality of fingers for electrical connections and a paddle for physical support."); '269 Patent at col. 1:41-44 ("the depressed positioning [of the paddle] will necessarily lead to a physical deformation of the paddle support arms during the forming process because the lead frame is initially a flat metal piece"); '269 Patent at col. 2:56-60 ("FIG. 2 is a top view of the single site . . . of a typical lead frame. Depicted are a lead frame site comprising an external mounting frame [labeled] 13, a paddle [labeled] 3, a plurality of fingers [labeled] 7, and a plurality of paddle support arms [labeled] 9 extending from the paddle."). Moreover, the Court's conclusion that the patentee intended to define the term "lead frame" as comprising not only the paddle, the support arms, and the fingers, but also the external mounting frame, is supported by the fact that both parties have proposed that the term "external mounting frame" should be defined as constituting a "portion of the lead frame." See Pl.'s Post-Hearing Brief at 38; Def.'s Post-Hearing Brief at 29.

As to the term "paddle," the Court finds that a construction which includes a reference to the paddle's relationship to a lead frame is unsupported by either the claim language or the specification. Atmel contends that such a reference is appropriate because, in practice, a paddle always exists, at least initially, within the context of a lead frame. See Def.'s Post-Hearing Brief at 28-29. Even if this contention is accurate as a practical matter, the claim language itself compels the conclusion that a person of ordinary skill in the art would understand the term "paddle" as it is used in the '269 patent to refer to the surface to which the chip is mounted

regardless of whether the paddle exists within the context of a lead frame or not. A comparison of the language in claim 1 and the language in claim 6 reveals that the patentee intended to cover "paddle support arms comprising a deformation absorbing member" not only (a) within the context of a paddle that is connected to an external mounting frame and that is part of a lead frame (as described in claim 1), but also (b) within the context of a paddle that is not connected to an external mounting frame and that is not part of a lead frame (as described in claim 6). In fact, the only apparent difference between claim 1 and claim 6 is precisely this absence in claim 6 of a reference to either a lead frame or an external mounting frame. Thus, it appears that the patentee in claim 6 specifically intended to cover deformation absorbing members even in the absence of an external mounting frame, in which case, even according to Atmel's own expert witness, it would be inaccurate to say that the paddle existed within the context of a "lead frame" (since a lead frame by definition includes an external mounting frame as discussed above). See Transcript of Hearing on December 6, 2002 ("Tr. 12/6/02") at 126.

The parties also dispute the proper construction of the term "external mounting frame." Atmel contends that the construction should include a reference to the fact that the external mounting frame is typically removed at a point in time subsequent to the depression of the paddle and the mounting of the chip. Again, although it may be true as a practical matter that the external mounting frame is typically removed at some point in time during the packaging process, the Court finds no basis in the intrinsic evidence for including this fact within the definition of the term itself.

The Court finds that the jointly-proposed construction of the term "paddle support arms" as "arms that support a paddle" is consistent with the intrinsic evidence of the '269 patent.

However, the jointly-proposed construction of the term "fingers" requires a slight modification in accordance with the notion, discussed above, that in the absence of an external mounting frame, the structure comprising the paddle (upon which the chip is mounted), the paddle support arms, and the fingers is not accurately referred to as a "lead frame." Thus, rather than construing "fingers" as "projecting pieces *of a lead frame* that are initially connected to the external mounting frame and that extend inward toward the center *of the lead frame* to facilitate electrical connections with a semiconductor integrated circuit chip," the Court will construe the term "fingers" as meaning "projecting pieces that are initially connected to the external mounting frame and that extend inward toward the center of *what is initially* the lead frame to facilitate electrical connections with a semiconductor integrated circuit chip."

In summary: (1) the term "lead frame" is construed as "the metal piece, initially flat, to which a semiconductor integrated circuit chip is mounted, and which comprises the external mounting frame, the paddle, the paddle support arms, and the fingers"; (2) the term "paddle" is construed as "the surface upon which a semiconductor integrated circuit chip is mounted"; and (3) the term "external mounting frame" is construed as "the exterior portion of the lead frame to which the paddle support arms and fingers are initially attached."

3. "deformation absorbing member"

Agere argues that the term "deformation absorbing member" should be construed as "at least one part of a paddle support arm that can localize deformation and maintain the desired physical characteristics of the paddle support arm." Atmel argues that the term "deformation absorbing member" should be construed as "a structure located on the paddle support arm(s) that performs the following functions at the following times: a) localizes deformation that may occur;

b) during paddle downsetting; and c) thereby maintains the desired physical characteristics." The only significant difference between these two constructions is the absence in Agere's proposed construction of a reference to the fact that the deformation that is sought to be "localized" is the deformation that occurs "during paddle downsetting." The only reason offered by Agere for the omission of this language is that the claim language already includes such a reference, and therefore including such a reference in the definition of "deformation absorbing member" would be redundant. If this reasoning were accepted, both proposed constructions would be wholly redundant and unacceptable, as all of the language in both constructions already appears in (and is in fact taken directly from) the claim language itself.

The Court generally agrees with the premise, implied in both parties' constructions, that the meaning of the term "deformation absorbing member" is clear from the face of the claim language itself, and the Court perceives no reason why including the language "during paddle downsetting" is any more redundant than a reference to "localizing deformation" or "maintaining desired physical characteristics." Therefore, the Court will adopt Atmel's proposed construction, with a slight modification for purposes of simplicity. The Court construes "deformation absorbing member" as "a structure located on a paddle support arm that localizes deformation during paddle downsetting and maintains desired physical characteristics."

4. "localizing deformation"

Agere argues that the phrase "localizing deformation" should be construed as "capable of collecting or accumulating in a specific area an alteration in form or shape." Atmel argues that the phrase "localizing deformation" should be construed as "accumulating or restricting the

deformation which occurs during the mounting step to the vicinity of the deformation absorbing member."

Agere offers no justification for including the term "capable" in the construction of this term, and the Court finds that it is unwarranted by the intrinsic evidence. As to the difference between Agere's use of the words "collecting or accumulating," and Atmel's use of the words "accumulating or restricting," the dispute appears to be disingenuous and unnecessary as both parties have relied upon a dictionary definition of the term "localize" as meaning "to collect or accumulate in or be restricted to a specific or limited area." See Webster's Third New Int'l Dictionary 1327 (1986). Furthermore, Agere's proposed construction refers to such localization occurring generally in *a* specific area, in accordance with the dictionary definition of the term "localize," while Atmel proposes that reference should be made to *the* specific area where such localization occurs, namely the vicinity of the deformation absorbing member.

It also appears that Agere has included within its proposed construction a definition of the term "deformation" ("an alteration in form or shape"), while Atmel has simply used the term "deformation" in its proposed construction without defining it. Finally, Atmel wishes to include a reference to the fact that such deformation occurs "during the mounting step," while Agere does not contend such a reference is necessary. The Court notes that the claim language itself does include a reference to the fact that the deformation in question occurs at a particular point in the process, but uses the language "during paddle downsetting," whereas the language proposed by Atmel, "during the mounting step," appears only in the specification. As it does not appear to the Court that the patentees intended this specification language to supercede the express

language in the claim, there is no reason to substitute the specification language "during the mounting step" for the claim language "during paddle downsetting."[10]

Thus, relying upon the significant degree of overlap between the parties' constructions, and based upon the reasoning set forth above, the Court will construe the term "localizing deformation" as follows: "collecting, accumulating, or restricting to a limited area, namely the vicinity of the deformation absorbing member, the deformation (or alternation in form or shape) that occurs during paddle downsetting."

5. "maintaining desired physical characteristics"

Agere argues that the phrase "maintaining desired physical characteristics" should be construed as "preserving the physical integrity of the paddle support arm." Atmel argues that the phrase "maintaining desired physical characteristics" should be construed as "preserving physical integrity of the paddle support arm by preventing a necked down region from forming." Clearly, the only significant difference between the two proposed constructions is Atmel's inclusion of the language "by preventing a necked down region from forming."

In support of its proposed construction, Atmel points to the patent description of Figure 2, where it is noted that as a result of the existence of the deformation absorbing member, "the desired electrical and physical characteristics are maintained after the forming operation as the paddle support arm does not form a necked down region." '269 Patent at col. 3:7-9. Atmel further refers to the testimony of its expert witness that he is unable to identify any physical phenomenon other than "necking down" which would constitute a potential threat to

[10] In fact, Atmel's own proposed construction of the term "deformation absorbing member" implicitly acknowledges that the deformation in question occurs, according to the claim language itself, "during paddle downsetting."

"maintaining desired physical characteristics." See Tr. 12/6/02 at 112. However, an expert witness's inability to conceive of, and the specification's lack of reference to, any other examples of a pertinent physical phenomenon which would constitute a potential threat to "maintaining desired physical characteristics" does not mean that such a limitation should be read into the claim language, which does not itself include any such limitation. See E.I. du Pont, 849 F.2d at 1433. Moreover, the specification expressly indicates that the patentee did not intend to limit the patent in this way. The Background of the Invention states: "The deformation *will generally be in the form* of a necking down, i.e., a constriction of paddle support arms in the transverse axial direction." '269 Patent at col. 1:44-46 (emphasis added). The description of Figure 2, which presents a deformation absorbing member that specifically prevents necking down, provides merely an example of the invention, and does not provide a sufficient basis for reading such a limitation into the claim language itself. Thus, the Court construes the phrase "maintaining desired physical characteristics" as "preserving the physical integrity of the paddle support arm."

6. "annular member"

Agere argues that the term "annular member" should be construed as "a member with both an internal hole and expanded dimensions in the direction perpendicular to the major axis of the paddle support arm, and with a hole in the member." Atmel argues that the term "annular member" should be construed as "a deformation absorbing member that is ring-like, with expanded dimensions perpendicular to the major axis of the paddle support arm."

First, Atmel's reference to an "annular member" as being "a deformation absorbing member" seems unnecessarily redundant since claims 4 and 9, in which the term "annular member" appears, clearly provide that the annular member *is* a deformation absorbing member.

See '269 Patent at col. 4:8-10 ("A package as recited in claim 1 in which said deformation absorbing member comprises an annular member."); '269 Patent at col. 4:34-46 ("A semiconductor integrated circuit package as recited in claim 6 in which deformation absorbing member comprises an annular member."). The only other significant difference between the parties' constructions is Agere's description of "an internal hole" as contrasted with Atmel's description of the member being "ring-like."

Atmel's description of the member being "ring-like" most closely comports with the only dictionary definition of the word "annular" offered by either party, which is "of, relating to, or forming a ring." Merriam-Webster's Collegiate Dictionary 47 (10th ed. 2001). However, in this case, the patentees clearly chose to be their own lexicographers, providing a specific definition for the term "annular member" in the specification. "In the embodiment depicted in FIG. 2, the deformation absorbing member 11 comprises an annular member, i.e., a member with expanded dimensions in the direction perpendicular to the major axis of the paddle support arm. The annular member is depicted as being circular although other shapes, e.g., oval, can be used." '269 Patent at col. 2:62-68. Moreover, there is no intrinsic or extrinsic evidence to support's Agere's description of the member having "an internal hole." Thus, although the word "annular" generally means "of, relating to, or forming a ring," the Court concludes that the term "annular member" as used in the '269 patent should be construed in accordance with the specific definition provided in the specification. Therefore, the term "annular member" is construed as "a member with expanded dimensions in the direction perpendicular to the major axis of the paddle support arm, which member may be, but need not necessarily be, circular or oval in shape."

IX. CONCLUSION

The foregoing constitutes the Court's construction of the claim terms disputed by the parties. A Claim Construction Order follows, as well as a Supplemental Order.

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF PENNSYLVANIA

AGERE SYSTEMS INC.,	:	CIVIL ACTION
Plaintiffs,	:	
	:	
v.	:	NO. 02-864
	:	
ATMEL CORPORATION,	:	
Defendant.	:	

CLAIM CONSTRUCTION ORDER

AND NOW, this day of May, 2003, upon consideration of the briefs, exhibits, supplemental filings, and oral argument presented by the parties in conjunction with the Markman hearing, it is hereby ORDERED that the meaning and scope of the patent claims asserted to be infringed and presented by the parties for construction are as follows:

THE '335 PATENT

1. "patterning" means "performing the process of lithography (producing a pattern that covers portions of the substrate with resist) followed by etching (selective removal of material not covered by resist) or otherwise transferring the pattern into the substrate."
2. "holes" means "hollow places in a solid body or mass."
3. "glue layer" means "a layer, composed of one or more materials, which is deposited prior to the tungsten and which has good adhesion both to the underlying dielectric layer and to the tungsten."
4. "covering" means "lying over and directly contacting."

5. "etching" means "the process for removing material in a specified area through a wet or dry chemical reaction, or by physical removal, such as by sputter etch."

6. "low pressure chemical vapor deposition" means "chemical vapor deposition that is carried out at pressures well below atmospheric pressure (760 torr), typically at pressures below approximately 2 or 3 torr."

THE '672 PATENT

1. "substrate" means "any underlying material or materials (such as a silicon wafer alone or a silicon wafer combined with other layers such as a dielectric layer) upon which other materials may be formed or deposited."

2. "function" is construed as a misspelling of the term "junction."

3. "self-limiting" means "exhibiting an effect that is characterized by a tungsten formation rate at 10 minutes that is less than 10% of the initial equilibrium rate."

4. "self-limiting thickness" means "the tungsten thickness achieved at 10 minutes under conditions in which a 'self-limiting effect' is achieved, *i.e.*, the tungsten formation rate at 10 minutes is less than 10% of the initial equilibrium rate."

5. 35 U.S.C. § 112, ¶ 6 applies to the claim language "wherein said deposition temperature and environment is controlled such that said interaction is self-limiting with a self-limiting thickness less than said junction depth" because this language recites a step-plus-function limitation, and this limitation is construed in accordance with the specification language at col. 3:56-67 of the '672 Patent.

THE ‘827 PATENT

1. “contact region” and “electrical contact region” both mean “an electrically conducting space or area to which another electrical conductor may be connected so as to allow current to pass.”
2. “semiconductor body” means “any semiconductor material.”
3. “opening” means “a hole, void, or open space.”
4. The claims do not require a particular sequence with regard to the steps of “heating in a non-oxidizing atmosphere” and “depositing a metal layer.”

THE ‘269 PATENT

1. “lead frame” means “the metal piece, initially flat, to which a semiconductor integrated circuit chip is mounted, and which comprises the external mounting frame, the paddle, the paddle support arms, and the fingers.”
2. “paddle” means “the surface upon which a semiconductor integrated circuit chip is mounted.”
3. “external mounting frame” means “the exterior portion of the lead frame to which the paddle support arms and fingers are initially attached.”
4. “fingers” means “projecting pieces that are initially connected to the external mounting frame and that extend inward toward the center of what is initially the lead frame to facilitate electrical connections with a semiconductor integrated circuit chip.”
5. “deformation absorbing member” means “a structure located on a paddle support arm that localizes deformation during paddle downsetting and maintains desired physical characteristics.”

6. “localizing deformation” means “collecting, accumulating, or restricting to a limited area, namely the vicinity of the deformation absorbing member, the deformation (or alternation in form or shape) that occurs during paddle downsetting.”

7. “maintaining desired physical characteristics” means “preserving the physical integrity of the paddle support arm.”

8. “annular member” means “a member with expanded dimensions in the direction perpendicular to the major axis of the paddle support arm, which member may be, but need not necessarily be, circular or oval in shape.”

BY THE COURT:

Legrome D. Davis

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF PENNSYLVANIA

AGERE SYSTEMS INC.,	:	CIVIL ACTION
Plaintiffs,	:	
	:	
v.	:	NO. 02-864
	:	
ATMEL CORPORATION,	:	
Defendant.	:	

SUPPLEMENTAL ORDER

AND NOW, this day of May, 2003, it is hereby ORDERED that Atmel may file an additional brief addressing only the two issues set forth below, by **June 23, 2003**, and that Agere may file a responsive brief by **July 14, 2003.** The parties may attach affidavits from their expert witnesses. The two issues to be addressed pertain to claim 1 of the '672 patent, specifically the following passage found at col. 7:2-6:

> "wherein said deposition temperature is chosen such that the yield of said junctions decrease not more than 10% compared to the yield obtained for the same [j]unction having a via aspect ratio of .75 and having a contact of only aluminum"

The two issues to be addressed are:

(1) whether the term "yield" is inadequately defined in the patent, thereby rendering claim 1 indefinite; and

(2) whether this claim language includes a "step-plus-function" limitation, and therefore falls within § 112, ¶ 6, and, if the claim does include a "step-plus-function" limitation, how this limitation should be construed.

BY THE COURT:

Legrome D. Davis